HIGH-EFFICIENCY 5-WATT POWER AMPLIFIER WITH HARMONIC TUNING

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ABSTRACT

An X-band power amplifier using harmonic tuning has demonstrated 36 percent power-added efficiency with 5 watts output power and 6.0-dB gain at 10 GHz. The key to this design is determining and matching the optimum load impedance for power-added efficiency at the first two harmonics.

INTRODUCTION

In conventional power amplifiers, the output of a common-source field effect transistor (FET) is presented with the optimum power load. To achieve higher power-added efficiency (PAE), the device is typically biased closer to pinch-off (Class B operation). This paper demonstrates an increase in the performance of gallium arsenide (GaAs) FET power amplifiers by increasing their efficiency through the use of harmonic tuning. The design method makes extensive use of nonlinear modeling.

DEVICE CHARACTERIZATION AND MODELING

The FET used in this amplifier is a Texas Instruments EG–9012 having a gate periphery of 1,200 μm and I_{dss} equaling 400 mA. This ion-implanted FET uses plated-through source via holes to minimize source inductance and increase heat-sinking capabilities.

The FETs were characterized at 10 GHz to determine the operating conditions that provide the highest PAE. Nine FETs from three slices were measured throughout a power sweep from small signal to saturation with nine different bias conditions. The bias conditions were V_d = 5, 7, and 9 volts and I_d = $I_{dss}/2$, $I_{dss}/4$, $I_{dss}/8$ with the current being set under small-signal conditions. For each bias condition and power level, both input and output were tuned for maximum gain.

The measurements provided a matrix of PAE and gain data for each FET at each power level and bias condition. From this data, the optimum bias conditions were found to be V_d = 7 volts and I_d = $I_{dss}/4$. With 20-dBm input power, the device exhibited 26.4-dBm output power and 44-percent PAE.

A nonlinear model is required to predict large-signal FET performance and to locate the optimum load impedances at the fundamental operating frequency and higher harmonics. The model used in this paper is based on the modified harmonic balance technique described by Peterson et al.(1) The equivalent circuit model for an FET used in this program is shown in Figure 1.

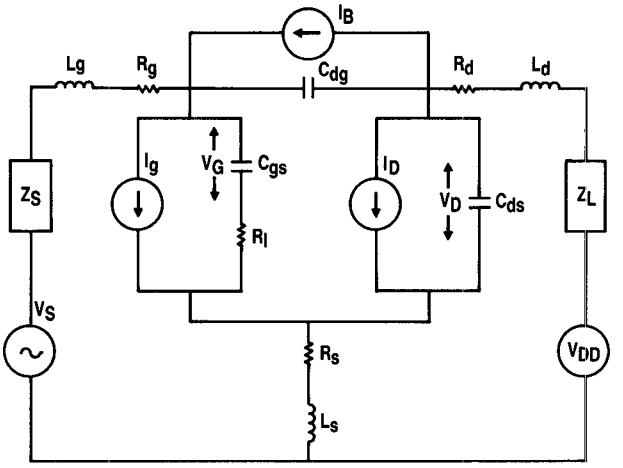

Fig. 1. Large-signal FET model

This large-signal model incorporates a standard small-signal FET model with the addition of three nonlinear current sources, I_D, I_G, and I_B. The current source I_D models the FET characteristic IV curves (this current source replaces g_m and R_{ds} of the small-signal model); current source I_B models the drain-source breakdown current; and I_G models the gate-source Schottky diode current. Current source (I_D) and the gate-drain breakdown current source (I_B) are measured on a 1-MHz pulsed IV setup described by Smith et al.(2) A typical diode curve is used for the gate-to-source (I_G) current source. Also included in the large-signal model are input and output (or load) networks. The small-signal elements of the model are determined through curve fitting of the s-parameters measured at the optimum bias conditions.

COMPUTER LOAD SEARCH

The typical procedure for designing power amplifiers requires data obtained from a load-pull measurement. A load-pull measurement locates the input and output loads for an

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FET that results in the highest output power. Circuits are then designed to match the impedances found from the load-pull measurement at the fundamental operating frequency of the amplifier, with little regard for the higher harmonic terminations. However, to truly maximize the large-signal performance of a device, it is also necessary to locate the optimum harmonic terminations. A means of accurately measuring the best harmonic terminations is currently unavailable. Therefore, to find these optimum harmonic-load impedances, an iterative search routine was performed using the large-signal model. The search routine, written in Fortran, stepped the output impedance in uniform increments around the Smith chart. At each impedance point, the gain and efficiency were simulated by the large-signal program. This iterative search began with the fundamental frequency and continued through the second and third harmonics. During the load-pull search, the input impedance of the FET was terminated with the small-signal conjugate match. The gain and efficiency calculations are accurate with this impedance match, as the input impedance of the FET was observed during measurements to be relatively insensitive to output mismatch and input power level. Table 1 shows the optimum harmonic loads found by the load search routine along with the gain and PAE at 10 GHz.

TABLE 1. SIMULATED GAIN AND EFFICIENCY AS HARMONIC LOADS ARE LOCATED ($f = 10$ GHz, $P_{in} = 20$ dBm).

Frequency (GHz)	Optimum PAE Load Impedance	Gain (dB)	PAE (%)
10	15 + j25.4	7.17	42.4
20	0 + j30.7	7.54	50.8
30	0 + j36.1	7.69	53.4

From Table 1 it is observed that if a circuit design can be found that matches the fundamental, second, and third harmonic load impedances, an improvement of 11 percent in PAE can be obtained compared with only matching the fundamental.

To verify the fundamental load found in the computer search, a load-pull test with tuners was initiated. Figure 2 shows the results of the computer load search where the second and third harmonics are optimally terminated; also shown is the best load found by the load-pull test. The lower efficiencies for the measured load-pull test are to be expected because of the lack of control over the higher harmonics.

CIRCUIT DESIGN AND RESULTS

To verify the predicted improvements in PAE, two single-stage FET amplifiers (0.5 watt and 5 watt) were designed with the goal of finding an output circuit topology that matched as closely as possible the first through third harmonics. Lumped-element impedance matching networks were used for the 0.5-watt design, and distributed element matching networks were used for the 5-watt design. Figures 3 and 4 show schematics of the two circuits that were developed.

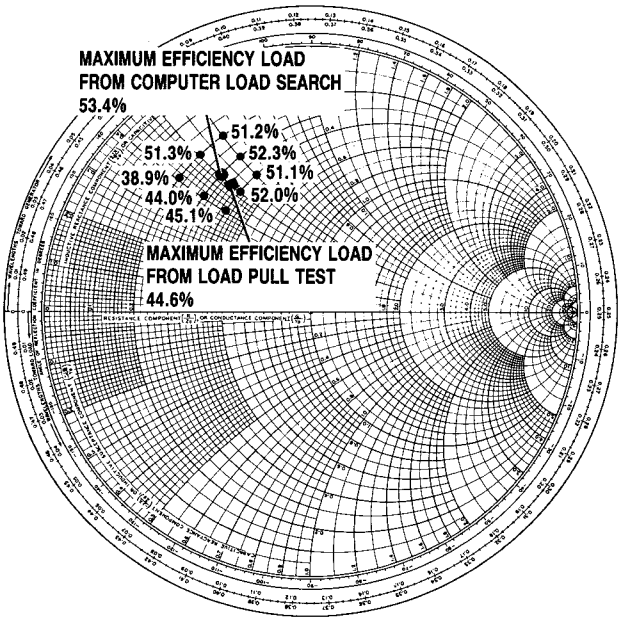

Fig. 2. Computer load-pull search

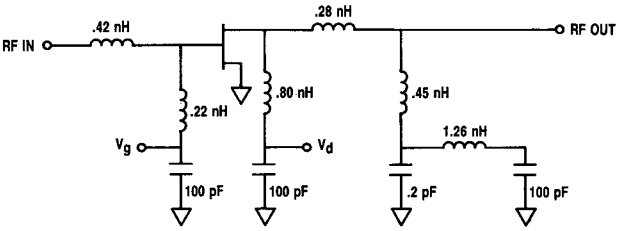

Fig. 3. 0.5-Watt amplifier schematic

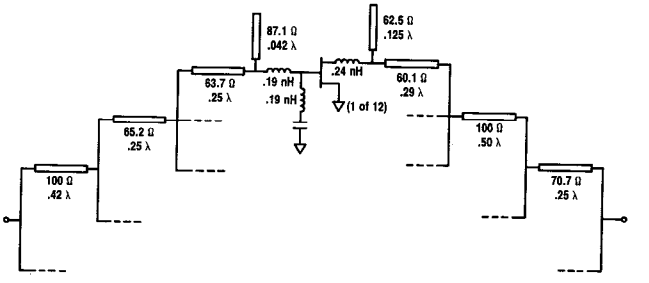

Fig. 4. 5-Watt amplifier schematic

Table 2 lists the computed harmonic loads for the circuit topology chosen for the 0.5-watt amplifier design as compared with the optimum loads. (Note: To keep the circuit at a reasonable complexity, the third harmonic was not optimally matched.) Figure 5 compares computed and measured performance of the 0.5-watt amplifier, and Table 3 lists the peak amplifier performance. The measured performance of this amplifier demonstrates the importance of matching the harmonic loads (not just the fundamental) in achieving an extra 10 percent in PAE.

TABLE 2. OUTPUT IMPEDANCE OF 0.5-WATT AMPLIFIER.

Frequency (GHz)	Load Impedance (Ohms) 0.5-Watt Amplifier	Computer Optimum
10	17.6 + j26.1	15.0 + j25.4
20	0.1 + j27.8	0.0 + j30.7
30	11.7 + j52.5	0.0 + j36.1

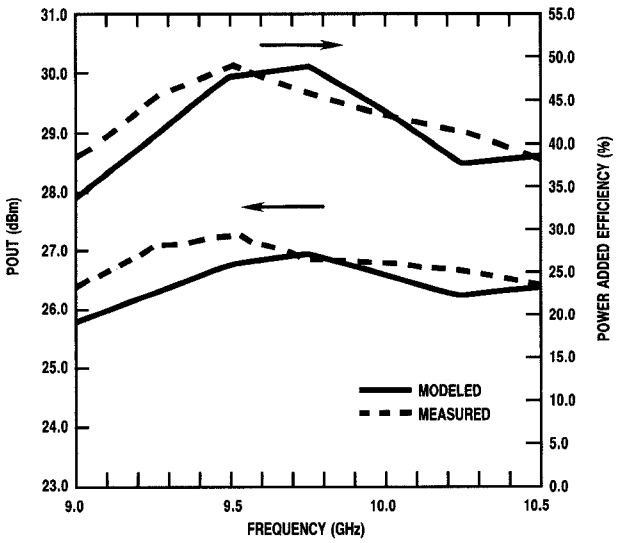

Fig. 5. 0.5-Watt amplifier performance

The successful demonstration of matching the optimum harmonic terminations in the 0.5-watt amplifier led to the design and fabrication of a 5-watt amplifier. Figure 6 is a photograph of the hybrid 5-watt amplifier. To achieve 5 watts of output power (including circuit losses in the combining networks) requires 12 EG–9012 1,200-μm FETs in parallel. The input and output matching networks are fabricated on 15-mil-thick alumina. The calculated and measured performance of this amplifier is shown in Figure 7. Table 3 includes the peak performance of the 5-watt amplifier.

TABLE 3. PERFORMANCE OF HIGH-EFFICIENCY POWER AMPLIFIER.

	0.5-Watt Amplifier	5-Watt Amplifier
Frequency (GHz)	9.75	10.00
PAE (%)	49.31	35.30
Pout (W)	0.51	5.27
Gain (dB)	6.04	6.22
Bias Conditions	V_d = 7.18 V I_d = 112.6 mA V_g = −2.25 V	V_d = 8.5 V I_d = 1.34 A V_g = −2.1 V

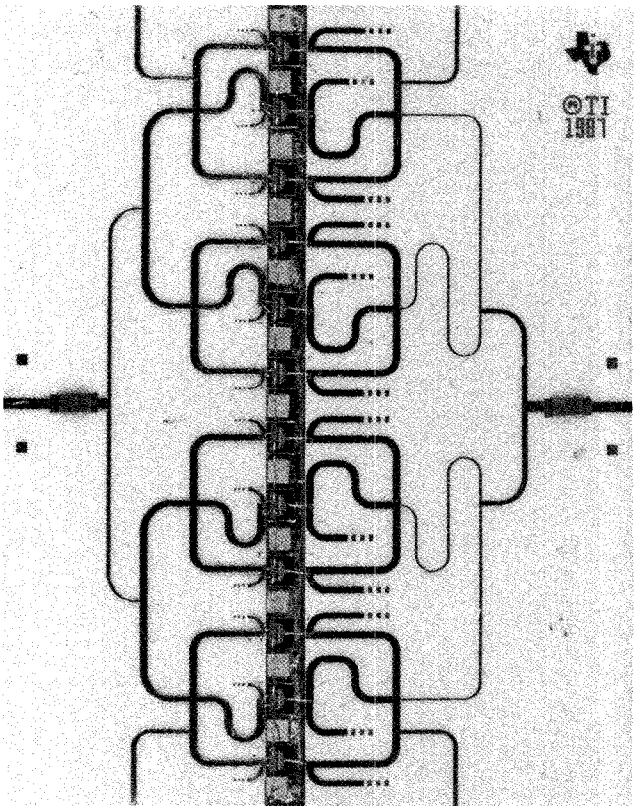

Fig. 6. 5-Watt amplifier photograph

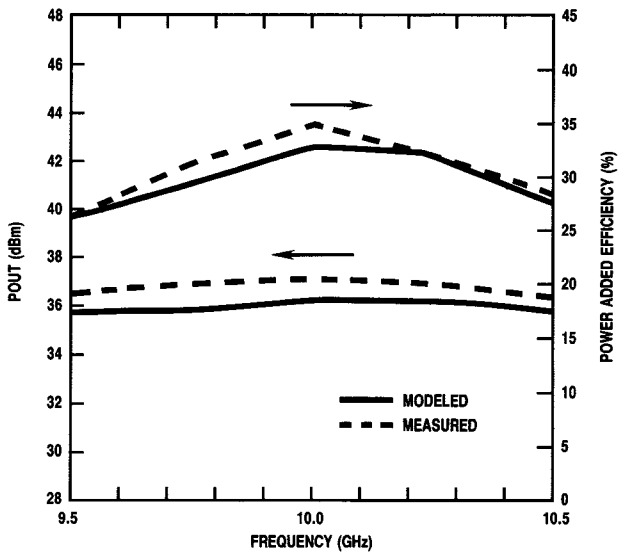

Fig. 7. 5-Watt amplifier performance

CONCLUSIONS

It has been shown that the efficiency of GaAs FET microwave power amplifiers can be increased through the use of harmonic tuning. Nonlinear models were used to study the effects of harmonic tuning and to determine the optimum harmonic terminations. Two amplifiers were designed that demonstrated high-efficiency power amplification at the 0.5-watt and 5-watt power levels. The effects of harmonic loading were demonstrated in the 0.5-watt amplifier, where the maximum efficiency measured for a device tuned only at the fundamental was 44.5 percent while the measured efficiency of the amplifier with optimum harmonic tuning was 49.3 percent.

ACKNOWLEDGMENT

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LIST OF REFERENCES

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[2] M.A. Smith, T.S. Howard, K.J. Anderson, and A.M. Pavio, "RF Nonlinear Device Characterization Yields Improved Modeling Accuracy," *1986 IEEE MTT International Microwave Symp. Dig.*, pp. 381–384.